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- 1 [Adaptive Message Logging for Incremental Replay of Message-Pass](#)
Robert H. B. Netzer, Jian Xu
May 1993 Adaptive Message Logging for Incremental Replay of Message-P
Publisher: Brown University
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Cyclic debugging is a common strategy where a program is executed ov
bugs. However, for message-passing parallel programs, cyclic debuggin
support of special tools. Variations in message latencies and process ...

- 2 [Parallel and vector computing: a practical introduction](#)
Ernst L. Leiss
April 1995 Parallel and vector computing: a practical introduction
Publisher: McGraw-Hill, Inc.
Additional Information: [full citation](#), [cited by](#), [index terms](#), [review](#)
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- 3 [CellSs: making it easier to program the cell broadband engine proce](#)
J. P. Perez, P. Bellens, R. M. Badia, J. Labarta
September 2007 **IBM Journal of Research and Development** , Volume 51 I
Publisher: IBM Corp.
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Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Citatio

With the appearance of new multicore processor architectures, there is
paradigms, especially for heterogeneous devices such as the Cell Broad
processor. CellSs is a programming model ...

- 4 [Superscalar multiprocessor design](#)
Mike Johnson
January 1991 Superscalar multiprocessor design
Publisher: Prentice-Hall, Inc.
Additional Information: [full citation](#), [index terms](#), [review](#)
Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Citatio
- 5 [Decoupled Software Pipelining with the Synchronization Array](#)
Ram Rangan, Neil Vachharajani, Manish Vachharajani, David I. August

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September 2004 **PACT '04**: Proceedings of the 13th International Conference on Architectural Support for Programming Languages and Compilation Techniques

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Full text available:  Pdf (311.44 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Bibliometrics: Downloads (6 Weeks): 6, Downloads (12 Months): 55, Citation (

Despite the success of instruction-level parallelism (ILP) optimizations in modern microprocessors, certain codes remain elusive. In particular, codes with complex control structure (RDS) traversal loops have been largely ...

6 [Address-indexed Memory Disambiguation and Store-to-Load Forwarding](#)

Sam S. Stone, Kevin M. Woley, Matthew I. Frank

November 2005 **MI CRO 38**: Proceedings of the 38th annual IEEE/ACM International Symposium on Microarchitecture

Publisher: IEEE Computer Society

Full text available:  Publisher Site ,  Pdf (301.30 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 33, Citation (

This paper describes a scalable, low-complexity alternative to the conventional load/store queue (LSQ) for superscalar processors that execute load and store instructions in parallel. It orders instructions prior to resolving their dependences. Whereas the ...

7 [Speculative hedge: regulating compile-time speculation against profiling](#)

Brian L. Deitrich, Wen-mei W. Hwu

December 1996 **MI CRO 29**: Proceedings of the 29th annual ACM/IEEE International Symposium on Microarchitecture

Publisher: IEEE Computer Society

Full text available:  Pdf (1.33 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 12, Citation (

Path-oriented scheduling methods, such as trace scheduling and hyperblock scheduling, extract instruction-level parallelism from control-intensive code by predicting important execution paths in the current scheduling ...

8 [Byte-code scheduling of Java programs with branches for desktop grids](#)

Eryk Laskowski, Marek Tudruj, Richard Olejnik, Bernard Tournal

November 2007 **Future Generation Computer Systems** , Volume 23 Issue 8

Publisher: Elsevier Science Publishers B. V.

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Citation (

A method for an introductory optimization of multithreaded Java programs on desktop grids is presented. It is composed of two stages. In the first stage, a clustering algorithm is applied to the program to identify ...

9 [Balance scheduling: weighting branch tradeoffs in superblocks](#)

Alexandre E. Eichenberger, Waleed M. Meleis

November 1999 **MI CRO 32**: Proceedings of the 32nd annual ACM/IEEE International Symposium on Microarchitecture

Publisher: IEEE Computer Society

Full text available:  [Publisher Site](#) ,  Pdf (1.50 MB) Additional Information: [full citation](#), [terms](#)

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 10, Citation (

Since there is generally insufficient instruction level parallelism within a performance is achieved by speculatively scheduling operations in super general because each branch competes for ...

Keywords: ILP compiler technique, lower bound, scheduling heuristic, completion time

10 [Trace scheduling: a technique for global microcode compaction](#)

[Joseph A. Fisher](#)

March 1995 Instruction-level parallel processors

Publisher: IEEE Computer Society Press

Additional Information: [full citation](#), [index terms](#)

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Citation (

Keywords: data dependency, global microcode optimization, microcode instruction scheduling, parallel processing, resource conflict

11 [Region Scheduling: An Approach for Detecting and Redistributing P](#)

[Rajiv Gupta, Mary Lou Soffa](#)

April 1990 **IEEE Transactions on Software Engineering** , Volume 16 Issue

Publisher: IEEE Press

Full text available:  [Publisher Site](#) Additional Information: [full citation](#), [abstract](#), [re](#)

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Citation (

Region scheduling, a technique applicable to both fine-grain and coarse-program representation that divides a program into regions consisting of level statements and permits the expression of both data ...

Keywords: coarse-grain parallelism, code generation, fine-grain, parallel compilers, program representation, reconfigurable long instruction word parallelism, region scheduling, scheduling., trace scheduling

12 [Low-power, low-complexity instruction issue using compiler assistance](#)

 [Madhavi G. Valluri, Lizy K. John, Kathryn S. McKinley](#)

June 2005 **ICS '05: Proceedings of the 19th annual international conference**

Publisher: ACM

Full text available:  Pdf (350.14 KB) Additional Information: [full citation](#), [abstract](#), [re](#)

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 43, Citation (

In an out-of-order issue processor, instructions are dynamically reordered in their data-ready order rather than their original program order to achieve logic that facilitates dynamic issue is one of ...

13 [A debugger for flow graph based parallel applications](#)

 [Ali Al-Shabibi, Sebastian Gerlach, Roger D. Hersch, Basile Schaeff](#)

July 2007 **PADTAD '07**: Proceedings of the 2007 ACM workshop on Parallel testing and debugging

Publisher: ACM

Full text available:  Pdf (344.87 KB) Additional Information: [full citation](#), [abstract](#), [re](#)

Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 49, Citation (

Flow graphs provide an explicit description of the parallelization of an application onto serial computations and edges onto message transfers. We present an implementation of a debugger for the flow graph based Dynamic ...

Keywords: flow graph based debugging, flow graph based parallel application detection, message reordering, parallel schedules

14 [Implicit parallelism with ordered transactions](#)

 Christoph von Praun, Luis Ceze, Calin Cascaval

March 2007 **PPoPP '07**: Proceedings of the 12th ACM SIGPLAN symposium on parallel programming

Publisher: ACM

Full text available:  Pdf (273.56 KB) Additional Information: [full citation](#), [abstract](#), [re](#)

Bibliometrics: Downloads (6 Weeks): 10, Downloads (12 Months): 101, Citation

Implicit Parallelism with Ordered Transactions (IPOT) is an extension of programming models to support speculative parallelization. The key idea is to parallelize a sequential program ...

Keywords: implicit parallelism, ordered transactions, parallel program thread-level speculation, transactional memory

15 [Trace Scheduling: A Technique for Global Microcode Compaction](#)

J. A. Fisher

July 1981 **IEEE Transactions on Computers**, Volume 30 Issue 7

Publisher: IEEE Computer Society

Full text available:  Publisher Site Additional Information: [full citation](#), [abstract](#), [c](#)

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Citation

Microcode compaction is the conversion of sequential microcode into efficient microcode. Local compaction techniques are those whose domain is basic block methods attack code with a general flow control. Compilation ...

Keywords: resource conflict, Data dependency, global microcode optimization compaction, parallel instruction scheduling, parallel processing

16 [Cache-efficient dynamic programming algorithms for multicores](#)

 Rezaul Alam Chowdhury, Vijaya Ramachandran

June 1998 **SPAA '08**: Proceedings of the twentieth annual symposium on parallel architectures

Publisher: ACM

Full text available:  Pdf (579.62 KB) Additional Information: [full citation](#), [abstract](#), [re](#)

Bibliometrics: Downloads (6 Weeks): 32, Downloads (12 Months): 234, Citation

We present cache-efficient chip multiprocessor (CMP) algorithms with g
used dynamic programming algorithms. We consider three types of caci
with a private cache for each core, *S-CMP* ...

Keywords: cache-efficiency, distributed cache, multicore, parallelism, s

- 17 [Maps: a Compiler-Managed Memory System for RAW Machines](#)
Agarwal Rajeev Barua Walter Lee Saman Amarasinghe Anant
July 1998 **Maps: a Compiler-Managed Memory System for RAW Machines**
Publisher: Massachusetts Institute of Technology
Full text available:  [Pdf](#) (101.55 KB) Additional Information: [full citation](#), [abstract](#), [re](#)

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 2, Citation C

Microprocessors of the next decade and beyond will be built using VLSI
transistors. In this generation of microprocessors, achieving a high leve
clock speed will require full distribution of ...

- 18 [A compilation technique for software pipelining of loops with conditio](#)
 Kemal Ebcioglu
September 1988 **SI GMI CRO New sletter** , Volume 19 Issue 3
Publisher: ACM
Full text available:  [Pdf](#) (677.33 KB) Additional Information: [full citation](#), [abstract](#), [re](#)

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 8, Citation C

We describe a compilation algorithm for efficient software pipelining of g
number of iterations and the time taken by each iteration may be unpre
then-else statements and conditional exit statements ...

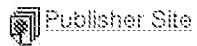
- 19 [An Approach to Platform Independent Real-Time Programming: \(1\) f](#)
Jozef Hoorman, Onno Van Roosmalen
July 2000 **Real-Time Systems** , Volume 19 Issue 1
Publisher: Kluwer Academic Publishers
Full text available:  [Publisher Site](#) Additional Information: [full citation](#), [abstract](#), [re](#)

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Citatio

A method for extending programming languages with timing constructs
specification of timing constraints in programs. The approach is not lang
extension can be included in many existing programming ...

Keywords: axiomatic semantics, compositional verification, distributed
independence, real-time programming

- 20 [Studying vertical dependence to improve NFS performance in wirele](#)
Cynthia D. Rais, Satish K. Tripathi
April 1998 **Cluster Computing** , Volume 1 Issue 2
Publisher: Kluwer Academic Publishers
Full text available: Additional Information: [full citation](#), [abstract](#), [re](#)



Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Citatio

Wireless networks experience a high level of errors and losses. These pl
have an impact on the performance of the higher layers. In addition, th
layer is contingent on the behavior ...

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